2017-05

Reduction of polymer residue on wettransferred CVD graphene surface by deep UV exposure

Suhail, A

10.1063/1.4983185
Applied Physics Letters
AIP Publishing

Reduction of polymer residue on wet–transferred CVD graphene surface by deep UV exposure

A. Suhail, K. Islam, B. Li, D. Jenkins, and G. Pan

Citation: Appl. Phys. Lett. **110**, 183103 (2017); doi: 10.1063/1.4983185
View online: http://dx.doi.org/10.1063/1.4983185
View Table of Contents: http://aip.scitation.org/toc/apl/110/18
Published by the American Institute of Physics

Reduction of polymer residue on wet–transferred CVD graphene surface by deep UV exposure

A. Suhail,[a] K. Islam, B. Li, D. Jenkins, and G. Pan
Wolfson Nanomaterials & Devices Laboratory, School of Computing, Electronics and Mathematics, Faculty of Science & Engineering, Plymouth University, Devon, PL4 8AA, United Kingdom

(Received 8 January 2017; accepted 26 April 2017; published online 4 May 2017)

Polymer residue from Polymethyl methacrylate (PMMA) on transferred graphene is a common issue for graphene devices. This residue affects the properties of graphene. Herein, we have introduced an improved technique to reduce the effect of this residue by deep UV (DUV) exposure of PMMA coated graphene samples within the wet transfer process. This technique has systematically been evaluated by optical microscopy, Raman spectroscopy, X-ray photoelectron spectroscopy, and electrical measurements. The results show that this residue is effectively reduced on the graphene surface after DUV treatment. In addition, the electrical characteristics of transferred graphene confirm that the sheet resistance and contact resistance are reduced by about 60 and 80%, respectively, after the DUV exposure. Electrical current transport characteristics also show that minimizing this residue on the graphene surface gives less hysteresis of electronic transport in back-gate graphene field-effect transistors. Furthermore, repeating electrical tests and aging shift the neutral point voltage of graphene. We attribute these improvements to cleaving of the chemical bonds in PMMA by DUV exposure and hence increasing the solubility of PMMA in acetone for subsequent processing steps. This work provides a unique route to enhance the electrical properties of transferred graphene after the fabrication process. *Published by AIP Publishing.*
[http://dx.doi.org/10.1063/1.4983185]

The attractive properties of graphene, such as near-zero bandgap, high electrical conductivity, high mobility, flexibility, and high transparency, have stimulated a lot of research interest.[1] One of the promising applications for graphene is in graphene field-effect transistors (GFETs). However, this device suffers from many issues such as open bandgap and doping of the graphene.[2] In addition, it is confirmed that the hysteretic phenomenon in this kind of device is highly dependent on the graphene surface and also ambient conditions.[3] Polymethyl methacrylate (PMMA) residue is one of the major issues that affect graphene surfaces after the wet-transfer process, which is used within the fabrication process of GFETs to transfer chemical vapour deposition (CVD)-graphene on desired substrates. This residue results in the shifting of the Dirac point, reducing the mean free path and mobility of carriers.[4] Moreover, it alters the electronic band structure of graphene when it is adsorbed at the edge or at defect sites.[5] Removing the residue of PMMA is a challenging issue for obtaining a graphene sheet with its intrinsic electronic properties.[6] There are many techniques used to reduce the effect of this residue such as a modified Radio Corporation of America (RCA) cleaning process. However, this technique requires the complicated wet chemistry and is limited to cleaning only a local area.[7] Formamide liquid (CH_3NO) has also been used to minimize the PMMA issue,[8] but this requires a long time (overnight) to deal with the PMMA issue. Other teams have tried to reduce this residue by using the annealing process in the forming gas at different temperatures. However, a systematic study of PMMA decomposition on graphene has proved that this technique cannot entirely remove the residue.[9]

In this work, we report an improved technique using deep UV treatment to effectively remove the PMMA layer from the transferred graphene surface and improve the properties of graphene. A systematic study of the current transport characteristic was carried out to investigate the hysteresis behavior in back-gate GFETs, which are fabricated with a width of 80 μm and two different channel lengths (90 and 190 μm). In addition, the effects of repeating the electrical test and aging process on the performance of fabricated devices are investigated.

The monolayer graphene was obtained from Graphene Supermarket (USA), and it was synthesized on both sides of 25 μm thick copper foil by the chemical vapour deposition (CVD) method.[10] The improved wet transfer process was used to transfer ultra-clean graphene onto SiO_2/Si substrates as follows. First, PMMA was dissolved in a chlorobenzene solution with a concentration of 10 mg/ml and spin-coated on one side of the graphene film at a spin speed of 4000 rpm for 30 s. Then, the sample was baked at 180 °C for 1 min. To etch the Cu substrate, DI water (DIW):HNO_3 at a ratio of 3:1 was used for 3 min followed by etching in 0.1 M ammonium persulfate for approximately 3 h with the endpoint determined when Cu was no longer visible. Afterwards, samples were etched for an additional 7 h in a separate fresh ammonium persulfate bath to ensure that the Cu was completely removed. The resultant PMMA/graphene membrane was transferred to a rinse bath of DIW for 20 min. Subsequently, monolayer graphene was directly transferred onto SiO_2/Si substrates. Before removing the PMMA layer, the samples

[a]Author to whom correspondence should be addressed. Electronic addresses: Ahmed.suhail@plymouth.ac.uk and ahmed.198381@yahoo.com

were irradiated with the deep UV (DUV) light of 254 nm at 180 °C for 20 min in air. During the irradiation process, a DUV lamp was fixed at a distance of 10 cm from the sample. Finally, a PMMA layer was removed by acetone treatment at 50 °C for 30 min followed by cleaning with IPA and DIW. Graphene on SiO_2/Si substrates obtained as such was dried in a vacuum before characterization and measurements.

To pattern graphene films by using an argon Plasma instead of an oxygen plasma, lift-off resist 3B (LoR) was spin-coated at 3000 rpm for 30 s on transferred graphene followed by the pre-baking at 175 °C for 15 min. Then, the photoresist was spin-coated at 4000 rpm for 30 s on the transferred graphene followed by pre-baking at 100 °C for 1 min. After creating patterns on the graphene film using the photolithography process, post-baking for prepared samples was achieved in an oven at 120 °C for 15 min. Subsequently, the argon plasma etching process at 50 W and 6×10^{-7} torr for 2 min is used to pattern CVD graphene. A heat sink sheet was placed underneath the device within the shaping process. The LoR and heat sink sheet were used to avoid the undesirable cross-link of the photoresist on graphene and enable the photoresist to be completely removed after the cleaning process. Samples were then treated with a remover at 60 °C for an hour followed by room temperature for 3 h. Then, samples were washed with DIW and vacuum dried. To form contact on graphene channels, the second photolithography using LoR and Photoresist was performed. Subsequently, the 5 nm Cr layer was thermally evaporated at 5×10^{-6} torr onto the graphene surface as an adhesion layer. Then, the 50 nm Au layer was sputtered at 6×10^{-7} torr on the top of Cr.

PMMA has been a well-known positive resist in advanced lithography.[11] The main mechanism for this process is the cleavage of chemical bonds for PMMA. Bond cleavage, in both the main chain and side groups, is the result of the absorption of high-energy radiation. For effective dissociation of PMMA, various radiation sources such as gamma rays,[12] x-rays,[13] electron beams,[14] proton beams,[15] and ion beams[16] have been used. Compared with all these methods, the DUV method excels in terms of simplicity and cost-effectiveness because DUV of 254 nm can be produced using inexpensive low-pressure mercury vapour lamps. The exposure of PMMA to DUV requires several hours at room temperature,[17] and very recently teams have used DUV treatment in combination with heating to reduced exposure dose to less than an hour.[18] Hence, in our current work, we have optimized DUV exposure of the PMMA layer within the wet transfer process to effectively remove this layer after acetone treatment. Under our optimized conditions, we practically found that the PMMA layer would be effectively removed. To evaluate the improved wet transfer process by the previously reported method,[10] after transferring graphene onto the desired substrate and drying process, the sample was baked at 220 °C for 5 min, and then the PMMA layer was removed by the acetone treatment. The quality and monolayer nature of transferred graphene were verified using an optical microscope. As shown in the optical image of Fig. 1(a), there are obvious spots of residual PMMA on the transferred graphene without DUV treatment. These spots affect the electrical properties of graphene and contact between the graphene and electrodes.[19] In contrast, Fig. 1(b) displays a typical optical image of transferred graphene with DUV treatment. It can be seen that the transferred graphene film was almost clean, uniform, and continuous. The monolayer nature of transferred graphene was evaluated by Raman spectroscopy as shown in Fig. 1(c). It can be observed from this figure that there is a peak for the D band in the spectrum of transferred graphene without DUV treatment at 1341 cm^{-1} that refers to some defects in monolayer graphene,[20] while the D-band is not observed in the spectrum of transferred graphene with DUV treatment. The intensity ratio of the 2D to G bands for transferred graphene by the developed technique was around 2, whereas it is about 1.6 for transferred graphene without DUV exposure. It is also clear from Fig. 1(c) that the Raman spectrum was red shifted after the DUV treatment, and this means that transferred graphene without the DUV treatment was p-doped due to the PMMA residue[21] and the PMMA residue was effectively minimized by DUV treatment. These characteristics indicated that the transferred graphene film using the DUV treatment was a high-quality monolayer.

X-ray photoelectron spectroscopy (XPS) (Kratos AXIS Ultra DLD spectrometer, monochromatic Al Kα emission at 1486.6 eV with an operating power of 150 W) was employed to further examine the amount of PMMA residue on the transferred graphene surface. Fig. 2 shows the C 1s core-level spectra of the transferred graphene with and without DUV treatment. As shown in Fig. 2(a), the spectral components attributed to the PMMA residue can be clearly observed in the spectrum of transferred graphene without DUV treatment, whereas XPS analysis showed a clear reduction in the intensity of these spectral components for transferred graphene using the DUV technique as illustrated in Fig. 2(b). This indicates that the PMMA residue was effectively minimized by this technique on the graphene surface.

The electrical characteristic of transferred graphene devices was studied using a Keysight B1500A semiconductor device analyzer in air at room temperature. The four-probe measurement was applied to determine the sheet resistance of the transferred graphene with and without DUV treatment onto SiO_2/Si substrates. The sheet resistance was in the range of $450 \pm 50\,\Omega\square^{-1}$ for the transferred graphene with DUV treatment, whereas it was in the range of $1150 \pm 50\,\Omega\square^{-1}$ for the transferred graphene without DUV treatment. These values are in agreement with those of graphene, transferred by PMMA and Scotch tape methods.[22] It is clear that minimizing the PMMA residue on graphene surfaces could reduce the sheet resistance by about 60% in comparison with untreated graphene. The contact resistance between graphene and electrodes is determined by the two-probe/four-probe method,[23] and it was around 118 and 600 Ω for transferred graphene with and without DUV treatment, respectively. It can be observed that the contact resistance of treated graphene is minimized by around 80% after DUV exposure. These results confirm that reducing the PMMA residue on the graphene surface will improve the electrical conductivity of graphene and contact between the graphene and electrodes.

To further investigate the transferred graphene, the hysteresis of graphene field effect transistors, which were fabricated with the same width of 80 μm and two length channels (90 and 190 μm), was measured in the ambient environment. The gate voltage was continuously applied through the

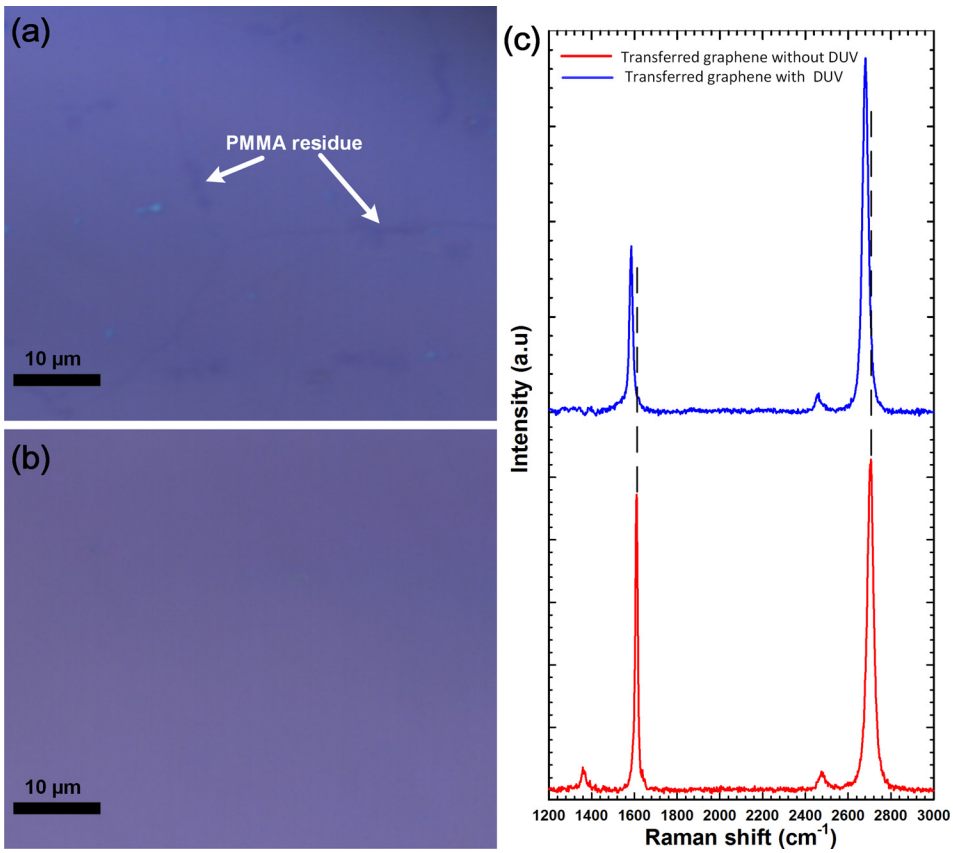

FIG. 1. (a) and (b) Optical images and (c) Raman spectrum of transferred graphene onto SiO_2/Si substrates without and with DUV treatment.

backside of devices from −40 to 0 V, then to +40 V, and back to −40 V. The source-drain bias (V_D) was constant at 0.1 V for all measurements. Fig. 3 shows typical (I_D-V_G) transfer curves of treated and untreated devices under forward and backward sweeps. The magnitude of hysteresis in these devices can be explained in terms of the difference in the threshold voltages $\Delta V_{th} = V_{thb} - V_{thf,}$ where V_{thf} and V_{thb} are the threshold voltages under forward and backward sweeps, respectively. The threshold voltages under both sweeps are obtained by extrapolating the linear region (ELR) method.[24] The ΔV_{th} values were 15(24–9) and 8 (29–21) V for untreated long and short channel devices, respectively, whereas ΔV_{th} values were 6 (4 + 2) and 1.2 (3–1.8) V for treated long and short channel devices, respectively. It is clear that the values of ΔV_{th} are reduced by 60 and 75% for treaded long and short channel devices, respectively, in comparison with those of untreated devices, which indicates that the number of trapped charges at the graphene/SiO_2 interface in untreated devices will be higher than that in treated devices. This reduces hysteresis in the I_D-V_G characteristics of devices treated with DUV (see Figs. 3(c) and 3(d)), compared with untreated devices as shown in Figs. 3(a) and 3(b). It can also be observed in Fig. 3 that Dirac points (neutral point voltages V_{np}) of devices were positively shifted under the backward sweep, and this shift is due to the electrical screening effect which originates from trapped charges at the graphene/SiO_2 interface.[25] In addition, it can be seen in this figure that V_{np} for short channel devices is more positively shifted than that for long channel devices. This is attributed to short-channel effects in GFETs.[26] The effect of repeating

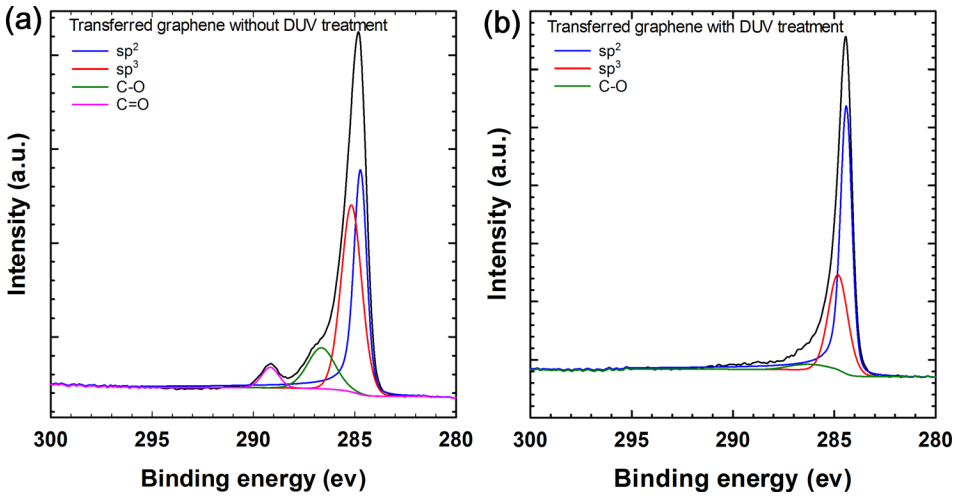

FIG. 2. XPS results of transferred graphene on SiO_2/Si substrates (a) without and (b) with DUV treatment, the black line represents the measured XPS spectrum, the blue line corresponds to graphene, and the others indicate PMMA residue.

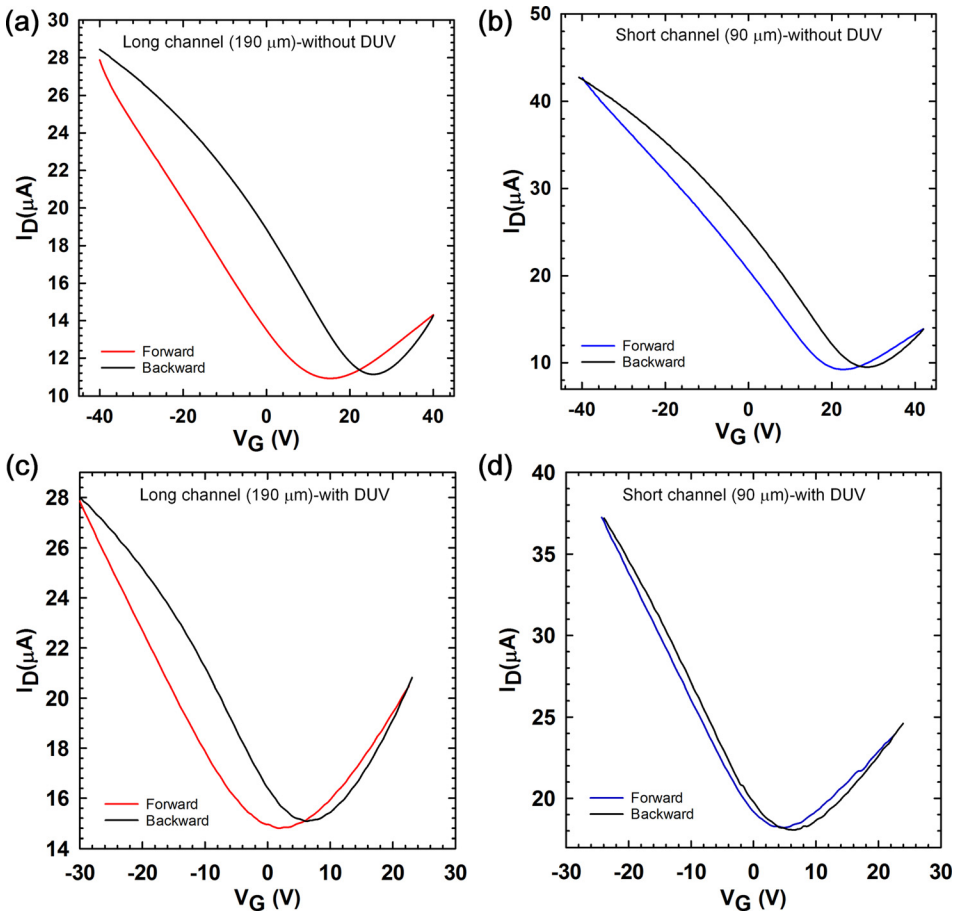

FIG. 3. Current – voltage (I_D-V_G) transfer curves measured in air at room temperature and $V_d = 0.1$ V under forward and backward sweeps. (a) and (b) Untreated long and short channel devices. (c) and (d) DUV treated long and short channel devices.

the electrical test on the treated long and short devices with DUV was also investigated under different recovery times (1, 10, 20, 50, 100, 200, and 500 s). This effect is explained in terms of shifted neutral point voltages under both sweeps as shown in Figs. 4(a) and 4(b). As can be observed in these figures, the V_{np} for both devices shifts with the recovery time under both sweeps. This indicates that the trapped charges at the graphene/SiO_2 interface have not completely been released after each test, and these charges will continuously accumulate and increase the electrical field screening effect for the next test. This behaviour will eventually lead to an increase in the shifting of V_{np}.[27] The values of the neutral point voltage differences ($\Delta V_{np} = V_{npb}$-V_{npf}) were reduced from 5 to 2.7 V for the treated short device and from 5.2 to 3.8 V for the treated long device after the recovery time of 500 s. This means that the number of trapped charges will be reduced, increasing the recovery time due to the limitation of interface trap sites at the interface. In addition, these devices showed less shifting of neutral point voltages when compared with those of published devices.[27] This confirmed that the treated GFETs would be more stable following repeated electrical measurements. The output characteristics of treated GFETs were also studied using the four-probe method in air at room temperature and V_g of 0 V as shown in Fig. 4(c). It can be seen that there is a linear relationship in $I_D - V_D$ curves for both devices, which suggests that there is an Ohmic contact between the graphene and the electrode. The calculated resistances in this figure were 0.56 and 1.18 KΩ for the short and long graphene channels, respectively.

The effect of aging on the performance of treated GFETs is also studied in terms of shifting neutral point voltages under the forward sweep, and these devices were left in the ambient environment without applying any voltage for a month. Fig. 4(d) displays the transfer characteristics of treated devices in air at room temperature and $V_D = 0.1$ V after aging process. As shown in this figure, there is a positive shift of V_{np} after the aging process, compared with those devices before the aging process (see Figs. 3(c) and 3(d)). It can be noticed that V_{np} was shifted from 2 to 23 V for the long channel device and from 5.5 to 21 for the short channel device after aging. It is clear that aging causes a shift in V_{np} and a decrease in the current (I_D). In addition, the V_{np} of long GFET was slightly higher than that of the short GFET, which suggests that the long channel device is more affected by an ambient environment due to the larger area of this device.

The reduction of the polymer residue is a key challenge in the fabrication of graphene devices. We have demonstrated the effect of the PMMA residue on the electrical and surface characteristics of graphene. Deep UV treatment for 20 min at 180 °C was employed within the wet transfer process to obtain clean, uniform, and continuous graphene, with typical low sheet resistance. In addition, the contact between graphene and electrodes was improved following DUV exposure. It was also confirmed that the hysteresis behavior in back-gate graphene field-effect transistors is minimized after reducing the PMMA residue. Furthermore, the treated devices showed more stability under repeating electrical tests during the recovery times, compared with untreated devices.

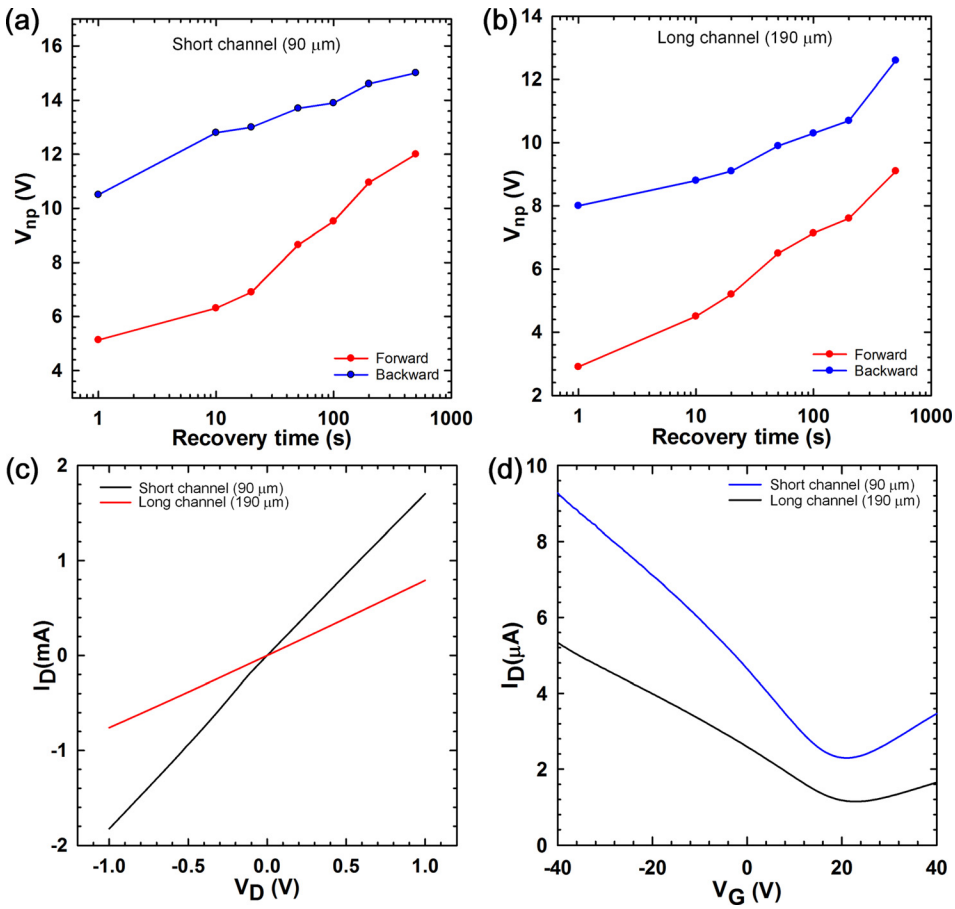

FIG. 4. (a) and (b) Shifting of neural point voltage of treated GFETs under repeating the electrical test at different recovery times in air at room temperature and $V_D = 0.1$ V. (c) Current – voltage (I_D-V_G) output curves of treated GFETs in air at room temperature and $V_G = 0$ V. (d) Current – voltage (I_D-V_G) transfer curves of treated GFETs measured in air at room temperature and $V_D = 0.1$ V after aging process.

Moreover, devices aged for a month exhibited an increase in the shift of the neutral point voltage of treated devices. We attributed the improvements in the performance of treated devices to cleaving of the chemical bonds in PMMA by DUV exposure and hence increasing the solubility of PMMA in acetone for subsequent processing steps. This work presents a viable and achievable approach for preparing low-cost, simple, and high-performance GFETs.

We acknowledge the financial support by The Higher Committee for Education Development in Iraq under the Grant No. D-11–2969.

[1]K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science **306**(5696), 666 (2004).
[2]H. Y. Chiu, V. Perebeinos, Y. M. Lin, and P. Avouris, Nano Lett. **10**(11), 4634 (2010).
[3]W. Kim, A. Javey, O. Vermesh, Q. Wang, Y. Li, and H. Dai, Nano Lett. **3**(2), 193 (2003).
[4]M. Ishigami, J. H. Chen, W. G. Cullen, M. S. Fuhrer, and E. D. Williams, Nano Lett. **7**(6), 1643 (2007).
[5]J. H. Chen, C. Jang, S. Adam, M. S. Fuhrer, E. D. Williams, and M. Ishigami, Nat. Phys. **4**(5), 377 (2008).
[6]Z. Cheng, Q. Zhou, C. Wang, Q. Li, C. Wang, and Y. Fang, Nano Lett. **11**(2), 767 (2011).
[7]A. B. Kuzmenko, E. V. Heumen, F. Carbone, and D. V. D. Marel, Phys. Rev. Lett. **100**(11), 117401 (2008).
[8]J. W. Suk, W. H. Lee, J. Lee, H. Chou, R. D. Piner, Y. Hao, D. Akinwande, and R. S. Ruoff, Nano Lett. **13**(4), 1462 (2013).
[9]W. Choi, Y. S. Seo, J. Y. Park, K. B. Kim, J. Jung, N. Lee, Y. Seo, and S. Hong, IEEE Trans. Nanotechnol. **14**(1), 70 (2015).
[10]X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, and E. Tutuc, Science **324**(5932), 1312 (2009).
[11]L. F. Thompson, C. G. Willson, and M. J. Bowden, *Introduction to Microlithography* (1983).
[12]H. Hiraoka, IBM J. Res. Develop. **21**(2), 121 (1977); H. Kudoh, N. Kasai, T. Sasuga, and T. Seguchi, Radiat. Phys. Chem. **48**(1), 95 (1996).
[13]H. Guckel, T. R. Christenson, K. J. Skrobis, D. D. Denton, B. Choi, E. G. Lovell, J. W. Lee, S. S. Bajikar, and T. W. Chapman, paper presented at the IEEE 4th Technical Digest on Solid-State Sensor and Actuator Workshop, 1990.
[14]W. Hu, G. H. Bernstein, K. Sarveswaran, and M. Lieberman, paper presented at the 2003 Third IEEE Conference on The Nanotechnology, IEEE-NANO 2003.
[15]K. A. Mahabadi, I. Rodriguez, S. C. Haur, J. A v. Kan, A. A. Bettiol, and F. Watt, J. Micromech. Microeng. **16**(7), 1170 (2006).
[16]M. B. H. Breese, G. W. Grime, F. Watt, and D. Williams, Nucl. Instrum. Methods Phys. Res., Sect. B **77**(1–4), 169 (1993).
[17]R. W. Johnstone, I. G. Foulds, and M. Parameswaran, J. Vac. Sci. Technol., B **26**(2), 682 (2008).
[18]L. Gammelgaard, J. M. Caridad, A. Cagliani, D. M. A. Mackenzie, D. H. Petersen, T. J. Booth, and P. Bøggild, 2D Mater. **1**(3), 035005 (2014).
[19]Y. Wang, C. Chen, X. Fang, Z. Li, H. Qiao, B. Sun, and Q. Bao, J. Solid State Chem. **224**, 102 (2015).
[20]K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J. H. Ahn, P. Kim, J. Y. Choi, and B. H. Hong, Nature **457**(7230), 706 (2009).
[21]A. Das, S. Pisana, B. Chakraborty, S. Piscanec, S. K. Saha, U. V. Waghmare, K. S. Novoselov, H. R. Krishnamurthy, A. K. Geim, and A. C. Ferrari, Nat. Nanotechnol. **3**(4), 210 (2008); C. Casiraghi, Phys. Rev. B **80**(23), 233407 (2009).
[22]H. Zhu, A. Liu, F. Shan, W. Yang, C. Barrow, and J. Liu, RSC Adv. **7**(4), 2172 (2017).
[23]W. Liu, J. Wei, X. Sun, and H. Yu, Crystals **3**(1), 257 (2013).
[24]J. J. Liou, A. O. Conde, and F. G. Sanchez, *Analysis and Design of MOSFETs: Modeling, Simulation, and Parameter Extraction* (Springer Science & Business Media, 2012).
[25]H. Wang, Y. Wu, C. Cong, J. Shang, and T. Yu, ACS Nano **4**(12), 7221 (2010).
[26]S. J. Han, Z. Chen, A. A. Bol, and Y. Sun, IEEE Electron Device Lett. **32**(6), 812 (2011).
[27]Y. Jie, J. Kunpeng, S. Yajuan, C. Yang, and Z. Chao, J. Semicond. **35**(9), 094003 (2014).